

REV1.0

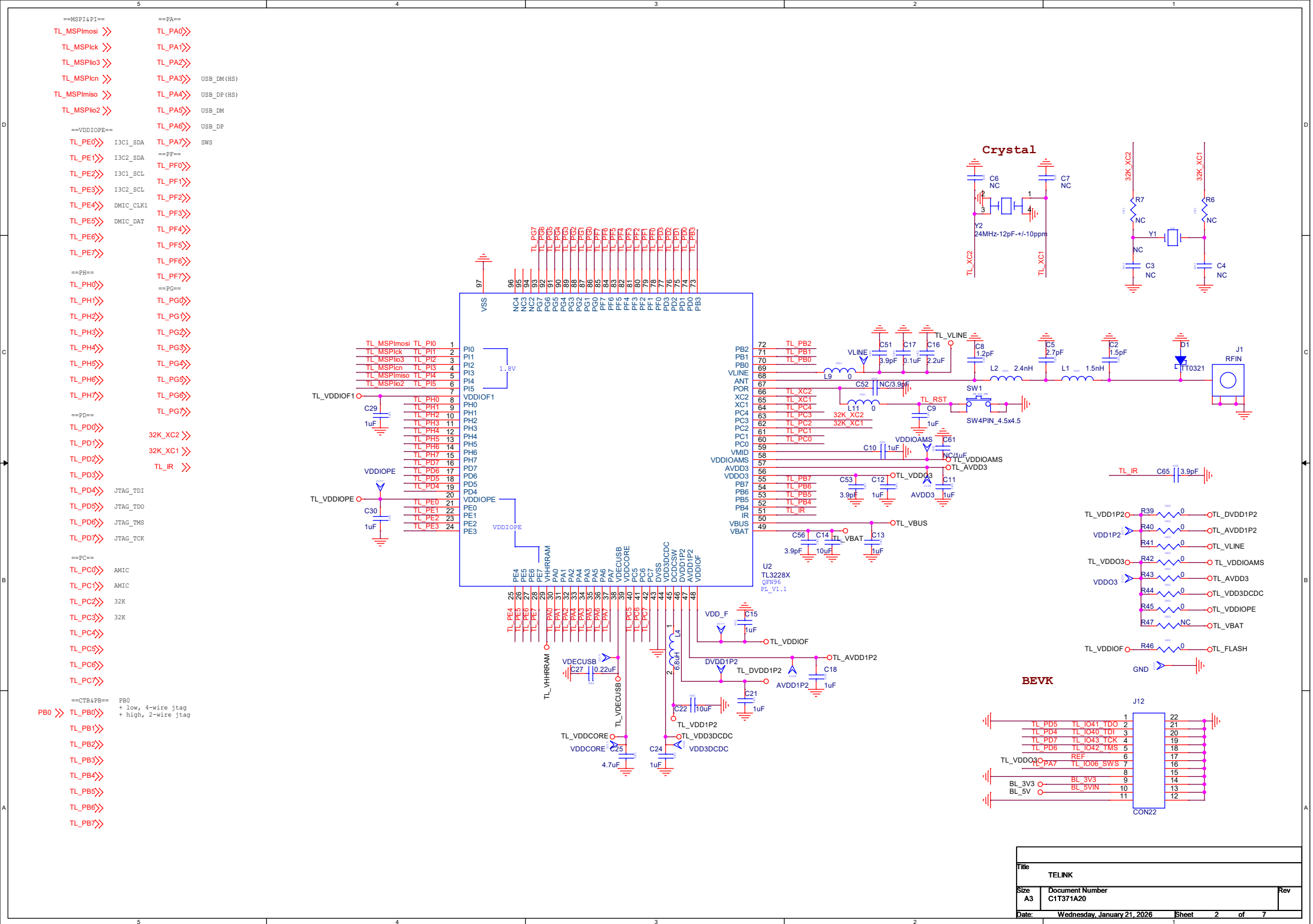
REV1.1

REV1.2

REV1.3

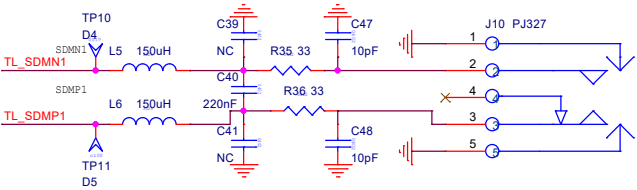
REV1.4

Author	Approved by		
zesheng	Xiang		
Date	Note		
2025/3/4	Initial Version		
2025/5/09	1.Add a jumper to connect TL_VDD3DCDC to VDDO3 2.Add a matching capacitor pad close to the chip side of the RF section 3.PCB Layout: Place the chip close to the antenna connector; remove the through-hole antenna connector 4.Change the power supply of AMIC to be from the GPIO port 5.Eliminate jumper connections for all peripheral power supplies and replace them with 0Ω resistor short-circuits 6.Change the PSRAM model to a 3.3V-powered version. 7.Change the REF signal of the JTAG debug port to VDDO3 8.Change the LED section to be directly driven by the GPIO port 9.Add PC0 and PC1 nets to connector J1 for adapting to the key sub-board 10.Modify the AMIC IO port configuration from PC0/PC1 to PC2/PC3 11.Simplify the IO port configuration of the I3C module 12.Modify the CTB section from the original PB0-PB7 to PC0-PC1 and PB2-PB7 13.Remove the test points for USB (HS) 14.Change the matching resistor of the CAN chip to 0805 package		
2025/7/25	1.Modify the board outline size to be consistent with that of other sold EVB versions; 2.Adjust the capacitance value of C58 from 4.7uF to 10uF; 3.Remove the entire PSRAM circuit; 4.Modify the pin definition of JTAG connector to adapt to NXP JTAG; 5.Remove the entire LIN circuit; 6.Remove the entire CAN circuit; 7.Remove the entire I3C circuit; 8.Remove the entire LCD screen circuit; 9.Remove the entire CTB circuit; 10.Modify the chip model of UART circuit to CH343P for a higher communication rate; 11.Modify the BEVK circuit to a module-based design.		
2025/12/02	A special test version is modified to verify all harmonic-related test items during the FCC certification process. (This version is exclusively for FCC harmonic test verification, not for regular development, promotion or demonstration.)		
2026/01/21	1.Correct the partial silk screen marking errors existing in the V1.2 version to ensure the accuracy and standardization of hardware markings; 2.Adjust the connection mode of TL_VDDO3 with TL_VDDIO_AMS, TL_AVDD3 and TL_VDD3DCDC: replace the original jumper connection with 0Ω resistor connection, and add corresponding test points for this link; 3.Adjust the connection mode of TL_VDD1P2 with TL_AVDD1P2, TL_DVDD1P2 and TL_VLINE: replace the original jumper connection with 0Ω resistor connection, and add corresponding test points for this link; 4.Optimize the design of partial signal traces, adjust the relevant traces to the inner layer of PCB, and improve the stability of signal transmission and the EMC performance of hardware.		

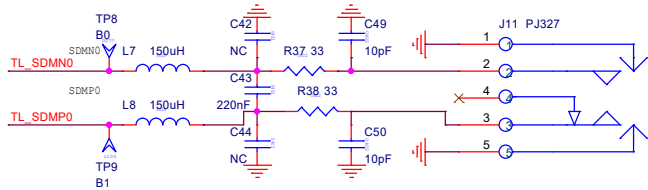


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TL_SDMP1 >>
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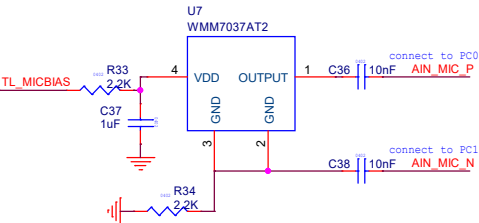
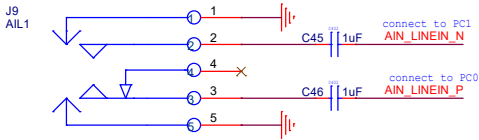
SDM1



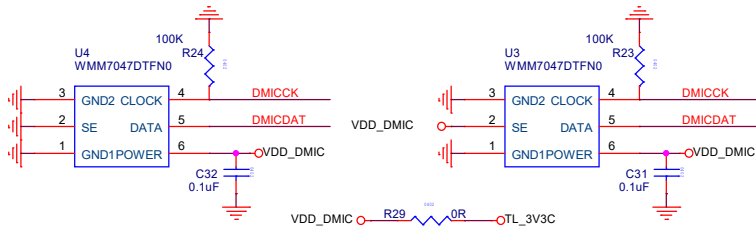
SDM0

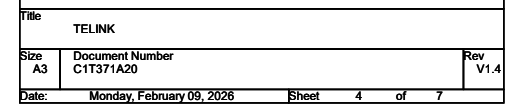


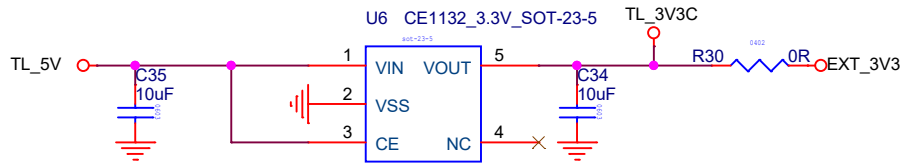
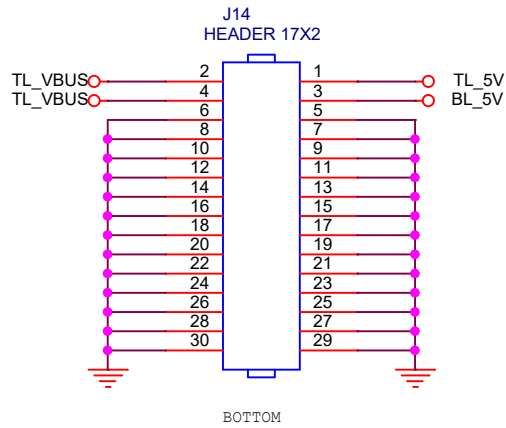
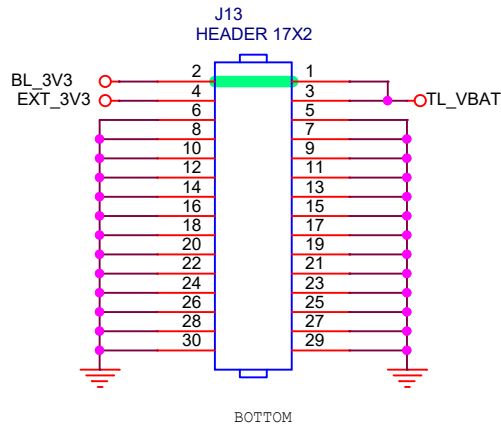
LINE IN & AMIC



DMIC







Title		
TELINK		
Size	Document Number	Rev
A4	C1T371A20	V1.4
Date:	Monday, February 09, 2026	Sheet 7 of 7