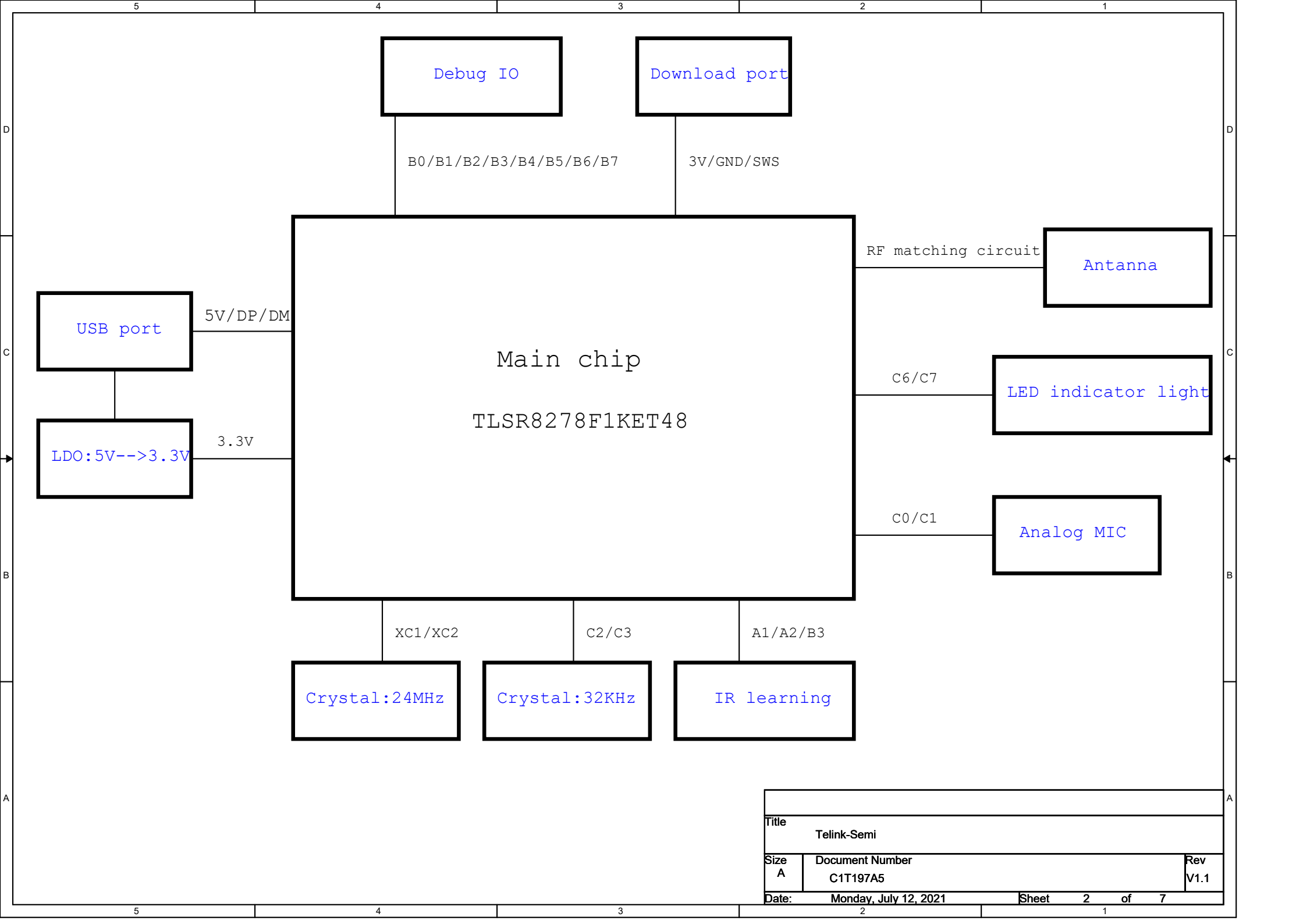


Date	Version	Note	Designer	Reviewer
2019-09-20	V1.0	Initial Version	Canlong	Lixiang
2019-10-16	V1.1	Update C2 from NC to 1.2pF Update L1 from 0R to 3nH Update C3 from NC to 2.2pF Update C8 from NC to 1.5pF	Canlong	Lixiang
2019-11-04	V1.1	CD1由220uF更为NC； Amic电路更为C1C0， 修改R7从4.7k更为0R C26 From1uF-->10nF	Zhenfei	Lixiang
2020-04-02	V1.1	Update value, C2=1.2pF L1=2.7nH C3=2.7pF Component manufacturer: Murata Chip log: TLSR8278F1KET48 ZHL2010 EP7945.41	Hongwei	Lixiang
2020-05-25	V1.1	Add block digram	Hongwei	Lixiang
2020-06-28	V1.1	Change DCDC inductor 4.7uH to 10uH	Hongwei	Weixiang
2021-07-12	V1.1	Add TVS diode TT0321SB to the RF pin, PCB is not updated	Hongwei	Weixiang
2023-10-09	V1.1	Add TVS diode TT0321SB/PESDRC2XP5VB to the RF pin, PCB is not updated Update value:L3=4.7uH	QIANG	Weixiang

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>>TL_DM [4]
>>TL_DP [4] >>TL_IROUT [6]
>>TL_Row0 [3] >>TL_IRin [6]
>>TL_Row1 [3] >>TL_IRcontrol [6]
>>TL_Row2 [3]
>>TL_Row3 [3]
>>TL_Row4 [3]
>>TL_Col0 [3]
>>TL_Col1 [3]
>>TL_Col2 [3]
>>TL_Col3 [3]
>>TL_Col4 [3]
>>TL_Col5 [3]
>>TL_C0
>>TL_AUDIO_C1

TP5 URX
TP6 UTX

TL_Row4 1
TL_Col1 2
TL_IRcontrol 3
TL_IRin 4
TL_Col4 5
TL_Col3 6
TL_DM 7
TL_DP 8
TL_SWS 9
TL_B0 10
TL_B1 11
TL_Col2 12

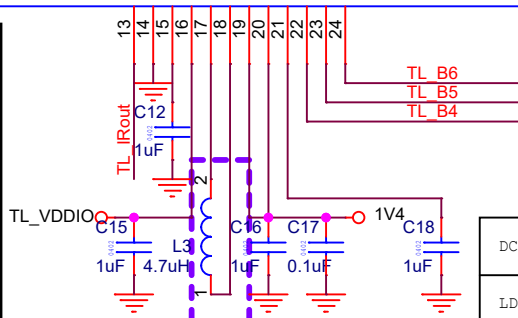
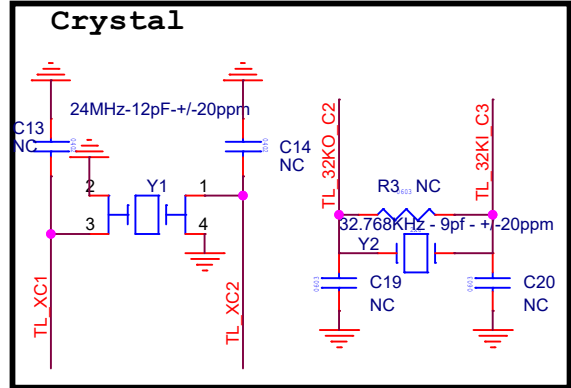
CK/SCL/I2SBCK/7816TRX/UTX/D[7]
DMIC_DI/P0N/URX/MDEC/A[0]
DMIC_CLK/7816CLK/I2SCLK/A[1]
DI/SDA/UCTS/P1/A[3]
CK/SCL/URTS/P2/A[4]
DM/A[5]
DP(SWS)/A[6]
SWS/URTS/A[7]
P3/URX/ATSEL1/MDEC/B[0]
P4/UTX/ATSEL2/B[1]
P5/UCTS/CYC2LNA/B[2]

P3N/URX/ATSEL0/C[5]
P2/UCTS/P0/C[4]
XC1
XC2
VMID
P1/URX/SCK/32KIN/C[3]
P0/7816TRX/UTX/SDA/32KO/C[2]
SCK/P1N/P0/audio_in/C[1]
SDA/P4N/URTS/MDEC/C[0]
VDD3
VBUS
SDMN1/DO/URX/B[7]

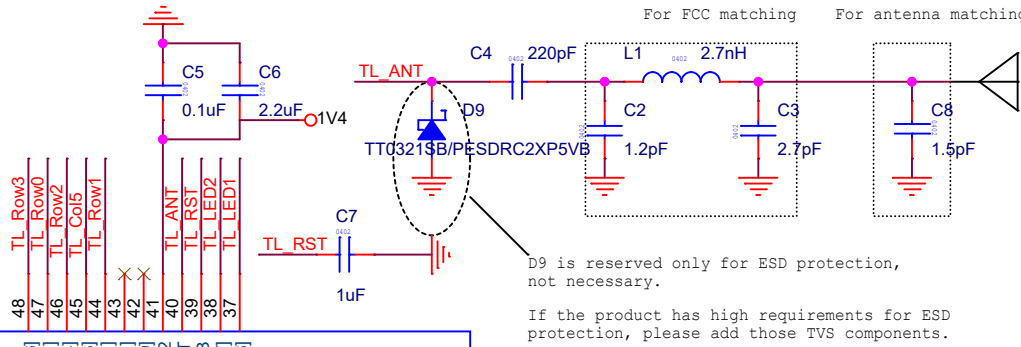
P0N/URTS/CYC2PA/B[3]
DVSS
VDD1V
VDD_IO
VDDC SW
VDDC SW
VDD1V2
AVDD1V2
VDD_F
SDMP0/P4/CMP_D/B[4]
SDMN0/P5/CMP_DF/B[5]
SDMP1/D/SDA/URTS/B[6]

TL_Col0 36
TL_XC1 35
TL_XC2 34
TL_32KI_C3 32
TL_32KO_C2 31
TL_AUDIO_C1 30
TL_C0 29
TL_VDD3 27
TL_VBUS 26
TL_B7 25

U1
TLR8278F1KET48

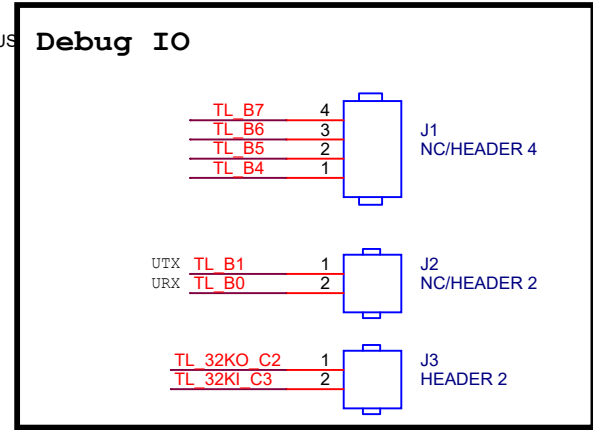
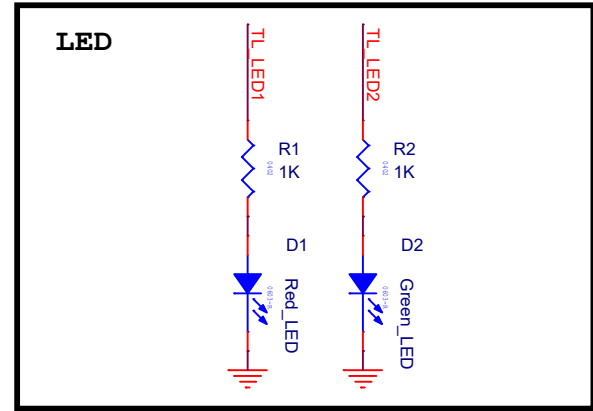
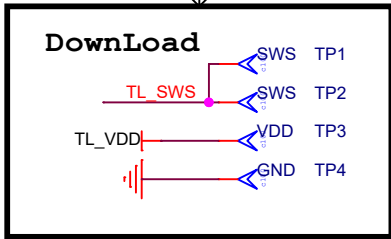


DC-DC MODE	L3=4.7uH
LDO MODE	L3=NC



RF

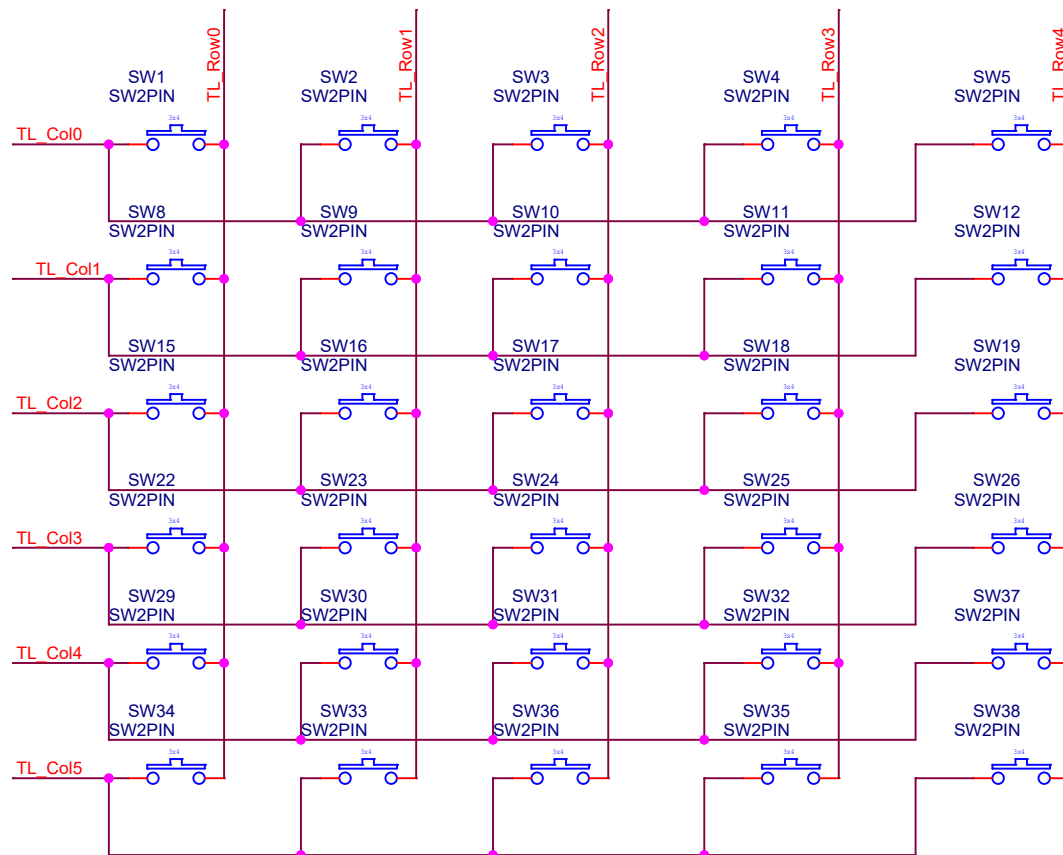
Jig 测试点



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>>TL_Row0 [2]
>>TL_Row1 [2]
>>TL_Row2 [2]
>>TL_Row3 [2]
>>TL_Row4 [2]

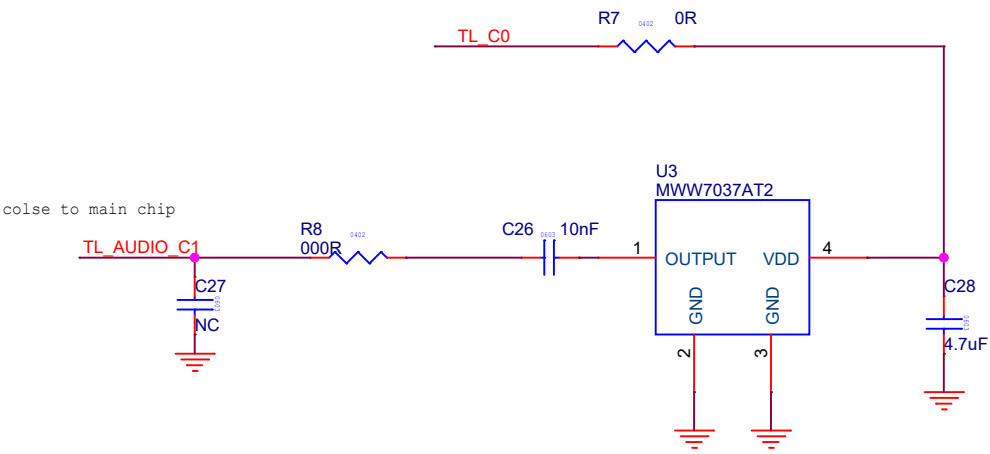
>>TL_Col0 [2]
>>TL_Col1 [2]
>>TL_Col2 [2]
>>TL_Col3 [2]
>>TL_Col4 [2]
>>TL_Col5 [2]



Please review multi-key processing section from customer specification,
and pay attention to schematics design in order to ensure that ghost
key dosen't occur while pressing multi-key

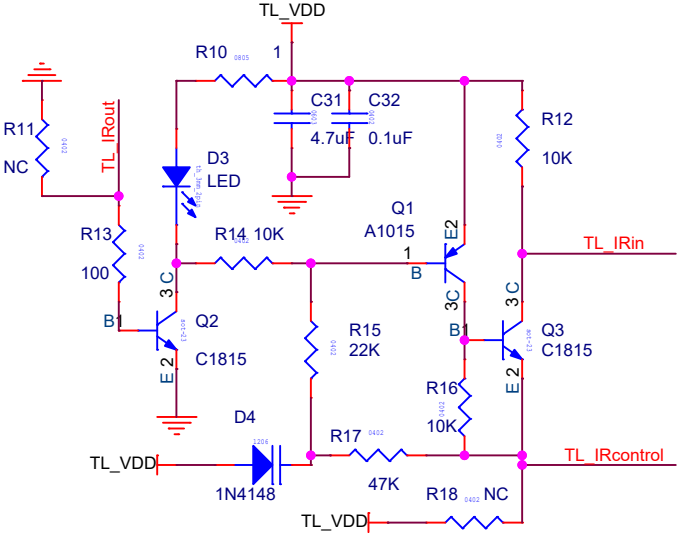
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>>TL_C0
>>TL_AUDIO_C1



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>>TL_IRout [2]
>>TL_IRin [2]
>>TL_IRcontrol [2]



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<Title>			
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