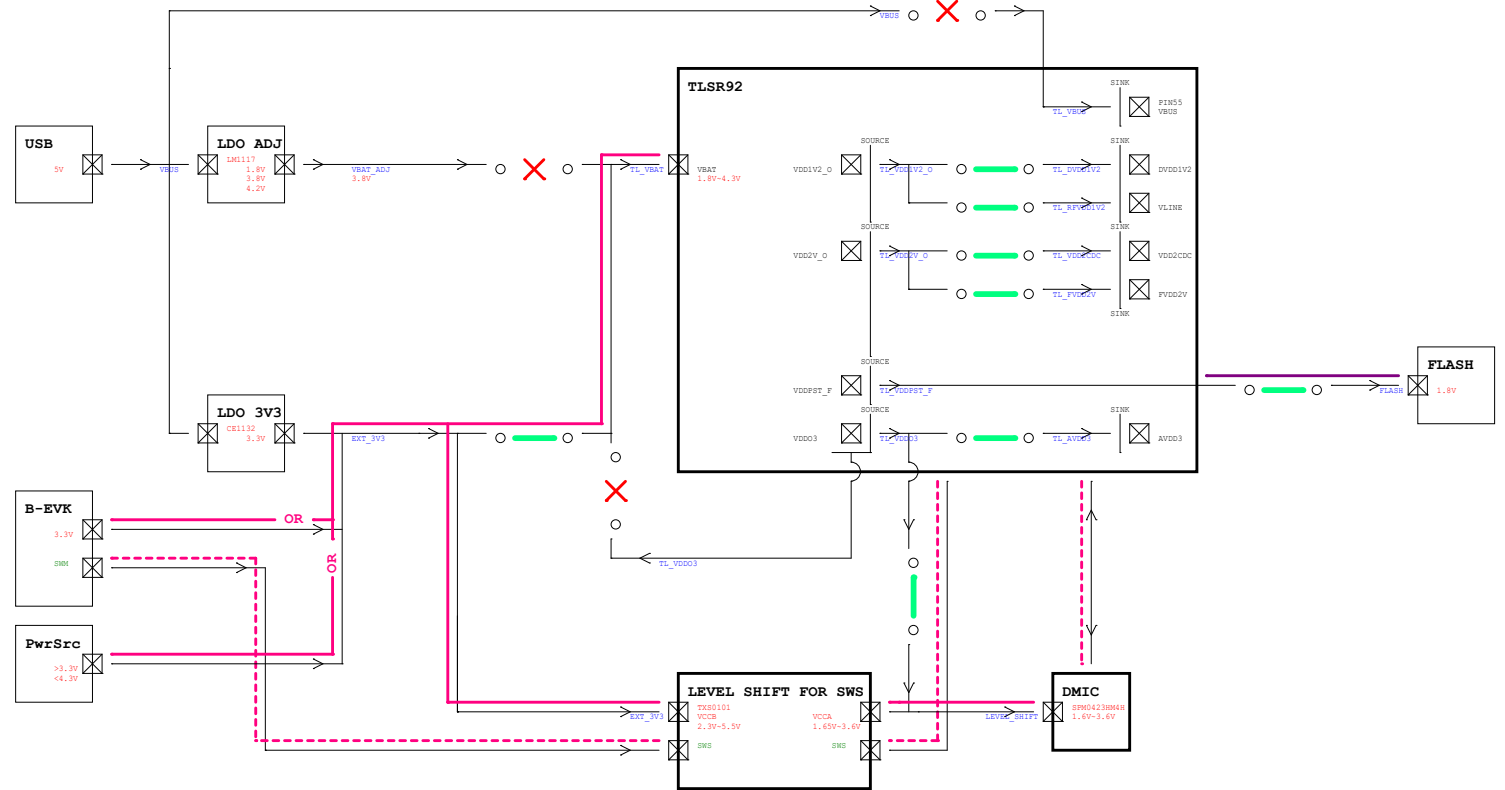


	Date	Note	Approved by	Reiwe
REV1.0	2023/05/31	Initial Version	zhangqiang	Jianbo weixiang
REV1.1	2023/07/28	1.TLSR9527BER QFN40E -> QFN40F 2.Remove PE6,control TL_KEY1 and LED_R by PE7,switching by jumper cap 3.Delete VDDPST TP test point and add S1 4.Modify J5,J16,J17,J21 pin assignments 5.Modify the supply voltage of U3 and U5 from EXT_3V3->LEVEL_SHIFT 6.Modify the VCCA pin of U8 from TL_VDDO3->LEVEL_SHIFT 7.Remove JTAG	HAIKUAN WU	Jianbo
REV1.2	2023/09/13	1.RF Ground revision: PIN30 GND and chip internal GND gap disconnected.		

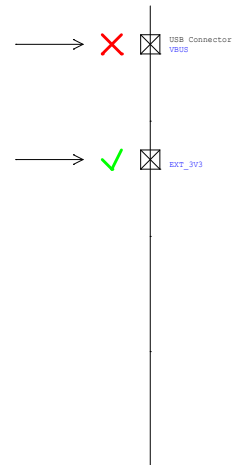
### 3.3V power domain SCENARIO-01

1. No USB plug-in.
2. Chip works under 3.3V power domain.
3. External power is connected to net of EXT\_3V3.
  - 3.1 External power range is from 3.3V to 4.3V.
  - 3.2 VCCB of level shift must be higher than VCCA of level shift.
  - 3.3 When uart or SWM is connected for communication, power supply must be set to 3.3V, since power domain of burning board is 3.3V.
4. Chip's power is from VBAT.

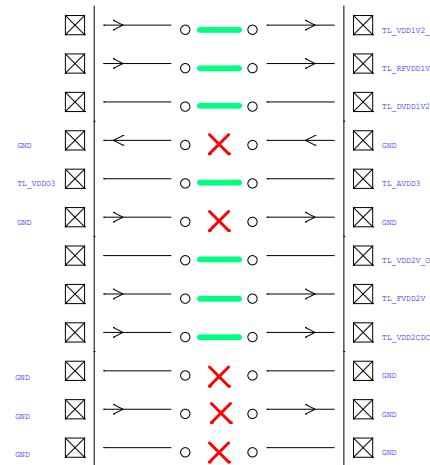


J15 AND U11

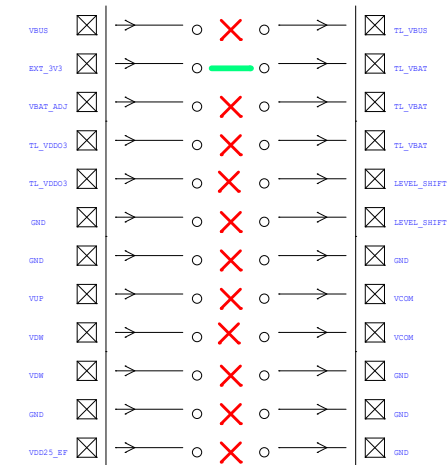
TOP VIEW



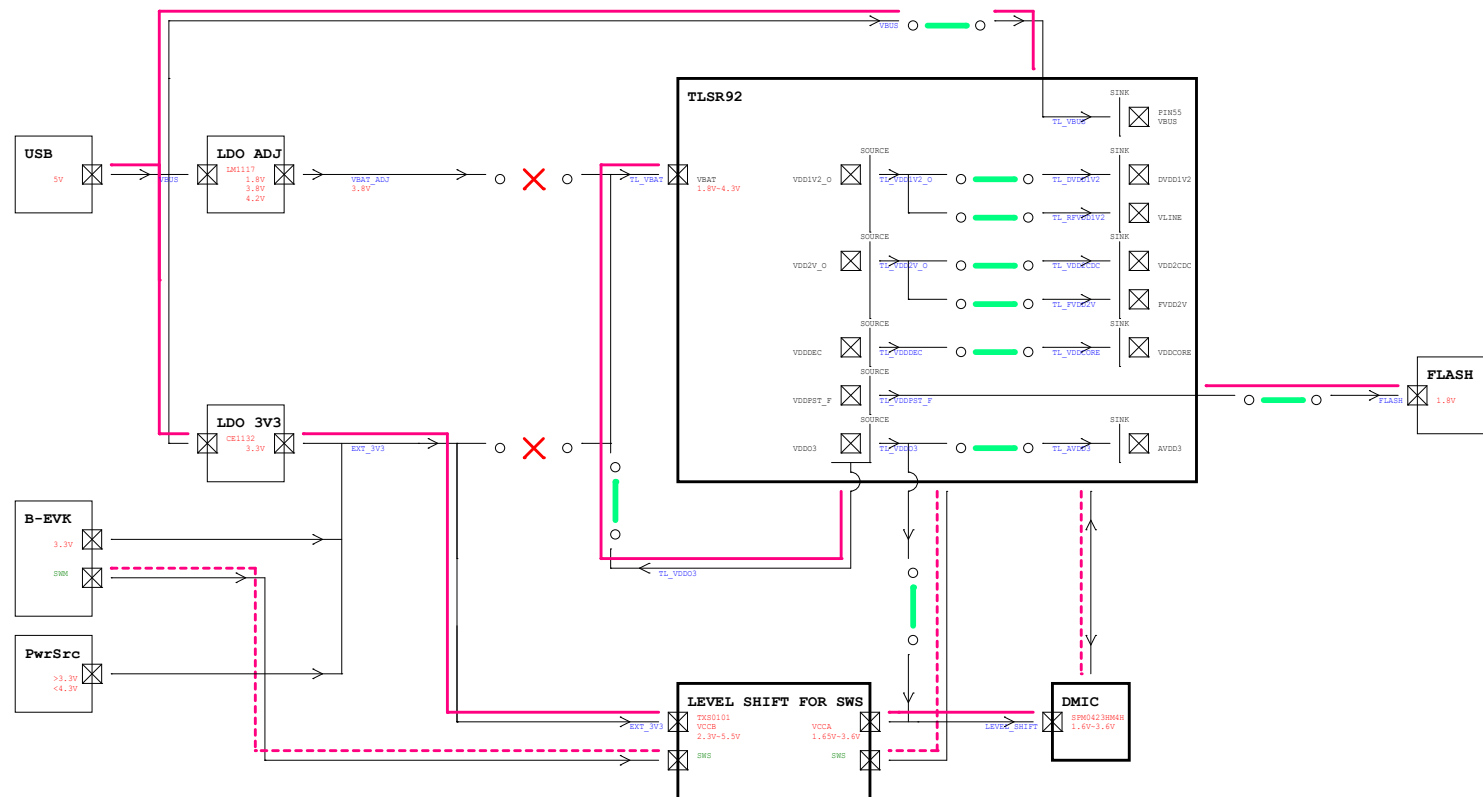
J16  
BOTTOM LEFT  
TOP VIEW



J17  
BOTTOM RIGHT  
TOP VIEW







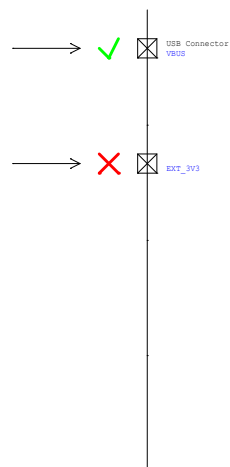
### 3.3V power domain SCENARIO-03:

1. USB plug-in, 5V is from USB connector.
2. Chip works under 3.3V power domain.
3. Chip's power is from VBUS.

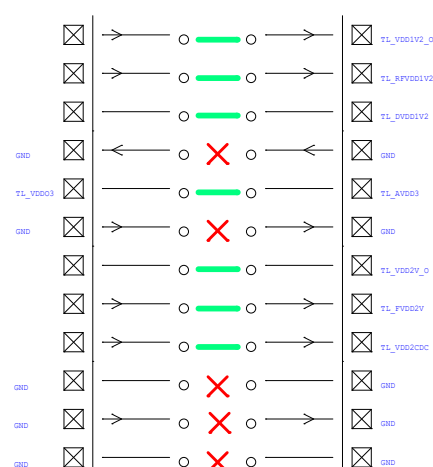
**Warning: just for verification, not for production.**

**J15 AND U11**

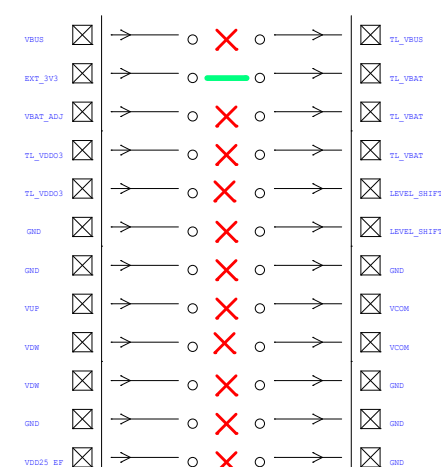
**TOP VIEW**

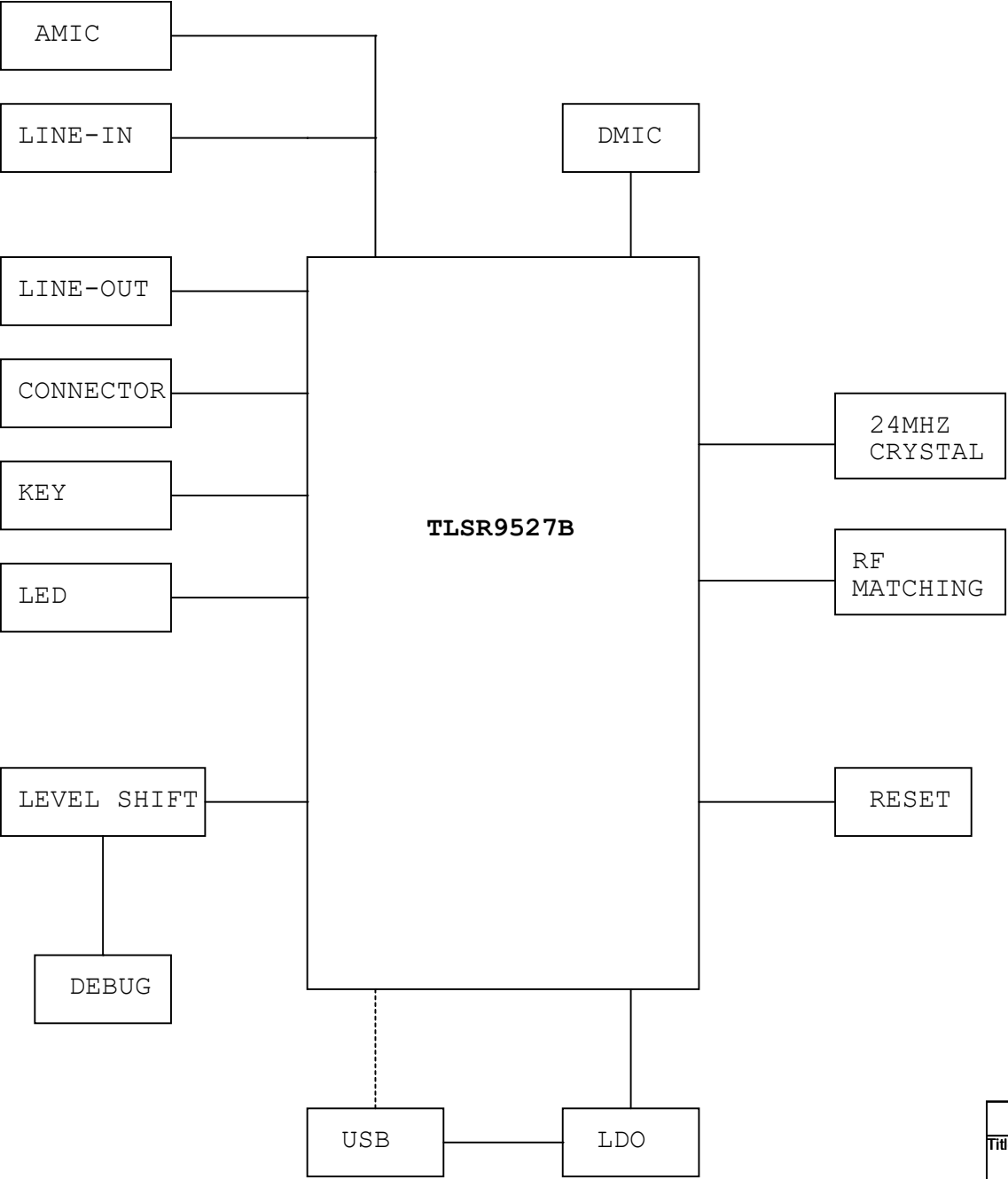


**J16  
BOTTOM LEFT  
TOP VIEW**



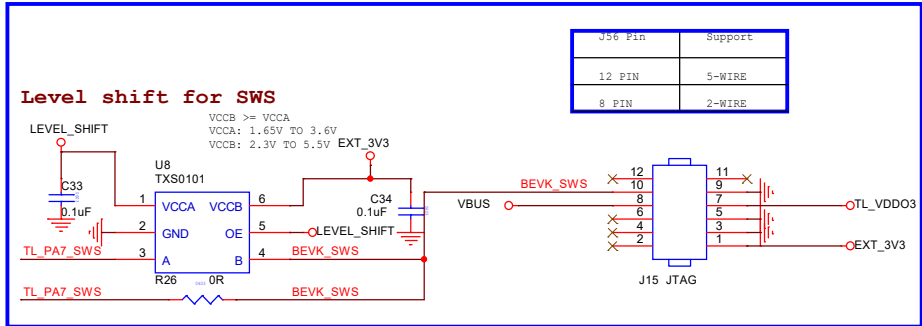
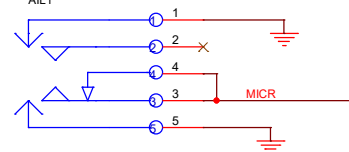
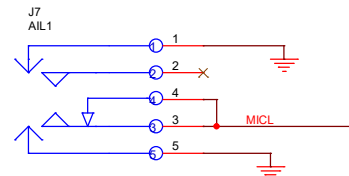
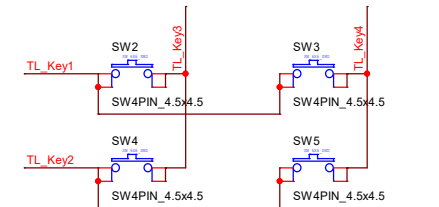
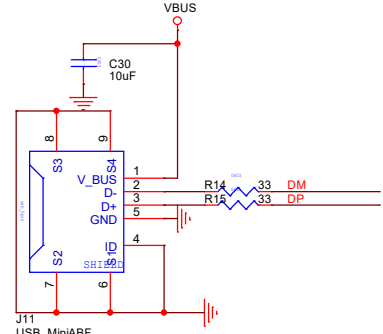
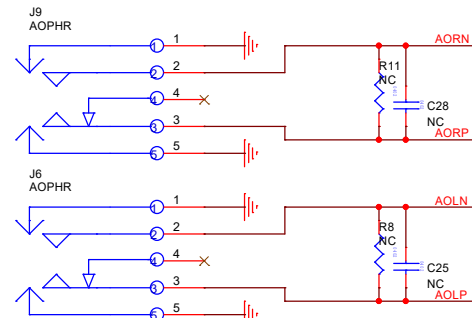
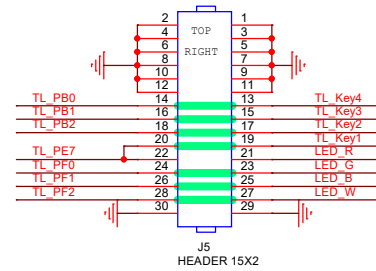
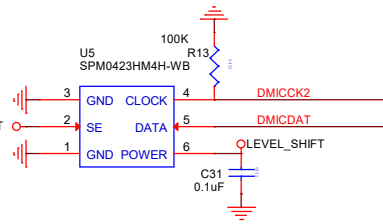
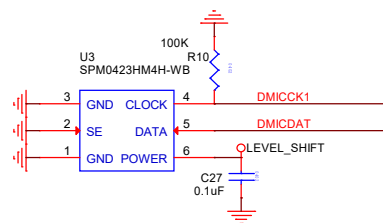
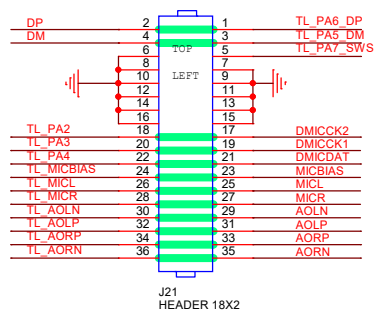
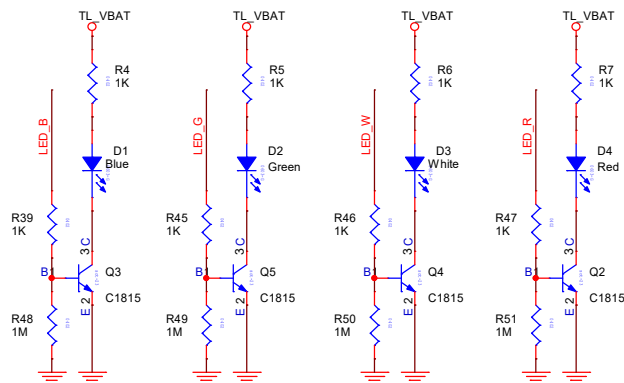
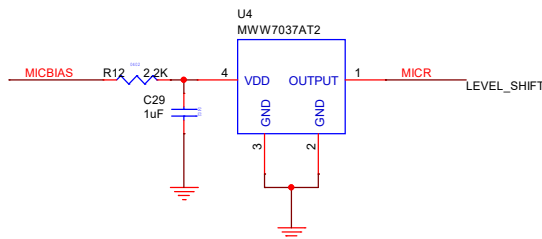
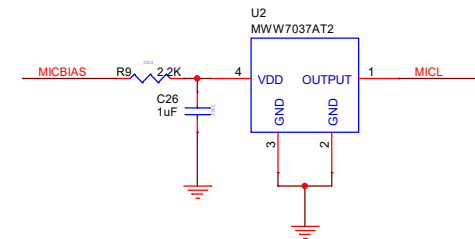
**J17  
BOTTOM RIGHT  
TOP VIEW**





Title		
TELINK		
Size	Document Number	Rev
A4	C1T289A20	V1.1
Date:	Friday, July 28, 2023	Sheet 2 of 5





J56 Pin	Support
12 PIN	5-WIRE
8 PIN	2-WIRE

