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Telink Qualification Report:- TLR9527BER

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Brief:

This document lists reliability test conditions and result of specified product, Guarantee the quality of products through relevant reliability tests.



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Revision History

| Version | Major Changes | Date | Author |
|---------|-----------------|------------|---------|
| 1.0 | Initial release | 2024/06/21 | Jie Ren |



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Reliability Qualification Report for TLR9527BER

1. Reliability test summary

| Stress | Total sample size | Number of Lots | Accept criteria | Test method | Test conditions |
|---------------------------|-------------------|----------------|--------------------|-------------------------|--|
| HTOL | 77 | 3 | 0 Fails | JESD22-A108 JESD85 | 125°C/1.1VCC/1000H |
| LTOL | 77 | 1 | 0 Fails | JESD22-A108 | -40°/1.1VCC/1000H |
| Preconditioning | 77*items | 1 | 0 Fails | JESD22-113 J-STD-020 | SAM-TC-Baking-Soaking-Reflow-SAM |
| Unbiased HAST with Precon | 77 | 1 | 0 Fails | JESD22- A118 | 130°C/85%RH /33.3psig/96hrs |
| PCT with Precon | 77 | 1 | 0 Fails | JESD22- A102 | 121°C, 100%RH, 205 kPa, 96hrs |
| TCT with Precon | 77 | 1 | 0 Fails | JESD22-A104 | -65°C to 150°C,0.5H/500cycle |
| HTSL | 77 | 1 | 0 Fails | JESD22-A103 | 150°C /1000hrs |
| SD | 15 | 1 | >95% lead coverage | JESD22-B102 | Steam aging:8H;245°C,5s |
| BPS | 30 bonds /5 units | 1 | CPK >1.67 | MIL-STD-883 | Characterization |
| BS | 30 bonds /5 units | 1 | CPK >1.67 | JESD22-B116 | Characterization |
| PD | 10 | 1 | CPK >1.67 | JESD22-B100/B108 | All dimensions |
| NVCE | 77 | 3 | 0 Fails | JESD22-117 | Ta=25°C/85°C,Vmax, 1k/10k/100k cycling |
| PCHTDR | 77 | 3 | 0 Fails | JESD22-117 | Ta=125°C, 500h |
| UCHTDR | 77 | 3 | 0 Fails | JESD22-117 | Ta=150°C, 1000h |
| LTDR | 77 | 3 | 0 Fails | JESD22-117 | Ta=25°C, Vmax,500h |
| ESD-HBM | pin combination*3 | 1 | 0 Fails | JESD22A-114 | ±2000V |
| ESD-CDM | 6 | 1 | 0 Fails | JESD22C-101 | ±500V |
| Latch-Up | 6 | 1 | 0 Fails | JESD78 | ±100mA/1.5*Vmax |

Moisture Sensitivity Level Test flow & Condition:

Electrical test → SAT → TC (-40 °C ~ 60 °C for 5 cycles) → Bake(125 °C ,24Hrs) →

Soaking Level 3 (30 °C,60%RH,192Hrs) → Reflow(260 °C,3 Cycles) → Electrical Test →

SAT



2 Introduction

In order to meet the most stringent market demands for high quality and reliability semiconductor components, Telink maintains a strict reliability program in all products. The purpose of this report is to give an overview of the reliability status of TLSR9527BER. Accelerated tests are performed on product, and then the results are extrapolated to standard operating conditions in order to calculate and estimate the component's failure rate.

3 Reliability

Many stress tests have been standardized in such documents as JESD471. From these standards, Telink has selected a series of tests to ensure that reliability targets are being met. These tests, including life test, environment test, ESD test and latch-up test, are discussed in the following sections.

3.1 Sample preparation Flow

CP → Assembly QFN40 → FT → Sampling Good Parts for Reliability test

3.2 Life test

The HTOL / LTOL test is configured to bias the operating nodes of the device samples. The devices may be operated in a dynamic operating mode. Typically, several input parameters may be adjusted to control internal power dissipation. These include: supply voltages, clock frequencies, input signals, etc., that may be operated even outside their specified values, but resulting in predictable and nondestructive behavior of the devices under stress. The particular bias conditions should be determined to bias the maximum number of potential operating nodes in the device. The HTOL test is typically applied on logic and memory devices. The LTOL test is intended to look for failures caused by hot carriers, and is typically applied on memory devices or devices with submicron device dimensions..

3.2.1 Test flow

HTOL Test Flow

B/I 168Hrs(125°C,1.1*Vint) → Electrical Test → B/I 500Hrs(125°C,1.1*Vint) →
Electrical Test → B/I 1000Hrs(125°C,1.1*Vint) → Electrical Test



LTOL Test Flow

B/I 168Hrs(-40℃,1.1*Vint) → Electrical Test → B/I 500Hrs(-40℃,1.1*Vint) →
Electrical Test → B/I 1000Hrs(-40℃,1.1*Vint) → Electrical Test

3.2.2 Test Criteria

| Test Item | Reference Standard | Test Condition | Test Times | Accept Criteria | Status |
|--------------|--------------------|----------------|------------|-----------------|--------|
| HTOL-1000Hrs | JESD22-A108 | Vcc=1.1*Vint | 1000hrs | 0/231 | Pass |
| | | Ta =125℃ | | | |
| LTOL-1000Hrs | JESD22-A108 | Vcc=1.1*Vint | 1000hrs | 0/77 | Pass |
| | | Ta =-40℃ | | | |

3.2.3 Failure Rate Calculation and Test Result

The life test is performed for the purpose of accelerating the probable electrical and physical weakness of devices subjected to the specified conditions over an extended time period.

Most integrated circuit failure mechanisms are based on physical or chemical reactions. These reactions are accelerated by temperature and can be modeled using the Arrhenius equation. The acceleration factor (AF) between any two temperatures may be calculated as follows:

:

$$AF_{(T_1-T_2)} = e^{\frac{Ea}{k}(\frac{1}{T_1} - \frac{1}{T_2})}$$

| Parameter | Description | Value |
|-----------|-------------------------------------|------------------|
| E | natural log | / |
| Ea | activation energy in electron volts | 0.7 eV |
| k | Boltzmann's constant | 8.62 x 10-5 eV/K |
| T1 | use temperature | 55℃ |



| | | |
|----|---------------------|--------|
| T2 | stress temperature | 125°C |
| AF | acceleration factor | 77.823 |

Next, a Chi square approximation of the mature life failure rate can be made using the following information:

$$\text{Failure rate (X}^2\text{)} = \frac{X^2_{(2f+2,\alpha)}}{2*n*T*AF}$$

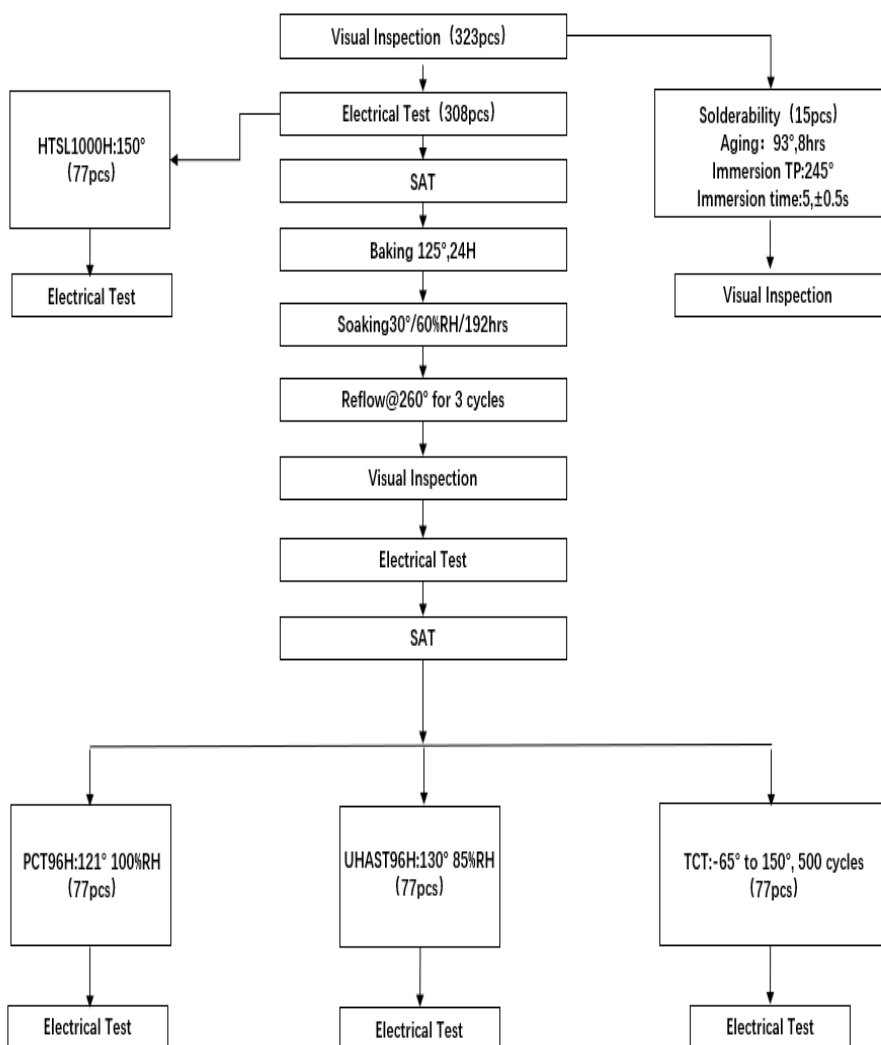
| Parameter | Description | Value | |
|-----------|-----------------------|---------------------------|---------------------------|
| f | number of failures | 0 | |
| α | 1 – confidence level | Confidence level 60% | Confidence level 90% |
| n | quantity tested | 231 | |
| T | test duration (hours) | 1000Hr | |
| AF | acceleration factor | 108.249 | |
| MTTF | Mean Time To Failure | 2.729*10 ⁷ Hr. | 1.086*10 ⁷ Hr. |
| FIT | Failure rate | 36.64 | 92.08 |



3.3 Environment Test

The purpose of environmental test is to evaluate the ability of semiconductor device to withstand the temperature stress, humidity stress, electrical stress or any combination of these. It can reveal not only the package quality issue but also the possible error in wafer process or chip design interacting with the assembly process.

3.3.1 Test Flow





3.3.2 Test Condition and Time

3.3.2.1 Moisture Sensitivity Test

The purpose of moisture sensitivity test is to identify the classification level of no hermetic solid state surface mount devices(SMDS) that are sensitive to moisture induced stress so that they can be properly packaged, stored, and handled to avoid subsequent thermal and mechanical damage during the assembly solder reflow attachment and/or repair operation.

| Test Item | Test Condition (Level III) | Test Time |
|-----------------------------|---|-----------|
| Temp. Cycle | -40°C ~ 60°C | 5Cycles |
| Bake | 125°C | 24Hrs |
| Unbiased Temp-Humidity Soak | 30°C, 60%R.H. | 192Hrs |
| Convection Reflow | <div><p>IR REFLOW PROFILE FOR 260 - 0 / +5°C (Pb-Free)</p><p>(a) Preheat Temp. = 60~120 seconds Max. (b) Temp. maintained above 217°C = 60~150 seconds (c) Temp. maintained above 230°C = 30~60 seconds (d) Temp. maintained above 255°C = 20~40 seconds (e) Peak Temp. Range = 260(-0/+5)°C & Max. 20 seconds P.S. Time 25°C to Peak Temp. = 8 minutes Max.</p></div> | 3Cycles |



3.3.2.2 High-Temperature Storage Life Test

The high-temperature storage life test measure device resistance to a high temperature environment that simulates a storage environment. The stress temperature is set to 150°C in order to accelerate the effect of temperature on the test samples. In the test, no voltage bias is applied to the devices.

| Test Item | Test Condition | Test Time |
|-----------|----------------|-----------|
| HTST | 150 °C | 1000Hrs |

3.3.2.3 Pressure Cooker Test

The pressure cooker test is an environment test that measures device resistance to moisture penetration and the effect of galvanic corrosion. The stress conditions for the pressure cooker are 121°C,100% relativity humidity, and 2.05atm pressure. Samples of surface mount devices are subjected to preconditioning and a final electrical test prior to the pressure cooker test

| Test item | Test Condition | Test Time |
|-----------|-----------------------|-----------|
| PCT | 121 °C,100%RH,2.05atm | 96Hrs |

3.3.2.4 Unbiased Highly Accelerated temperature and humidity Stress Test

The unbiased highly accelerated stress test is performed for the purpose of evaluating the reliability of non-hermetically packaged solid-state devices in humid environments. It employs temperature and humidity under non-condensing conditions to accelerate. The stress condition of the HAST are 130 °C,85% relativity humidity,2.3atm pressure. Samples of surface mount devices are subjected to preconditioning and a final electrical test prior to the highly accelerated temperature and humidity stress test.

| Test item | Test Condition | Test Time |
|-----------|------------------------------|-----------|
| UHASt | 130 °C,85%RH,2.3atm,unbiased | 96Hrs |

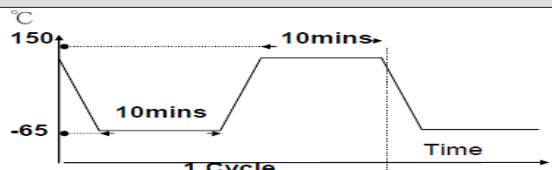
3.3.2.5 Temperature Cycling Test

The purpose of temperature cycling test is to study the effect of thermal expansion mismatch among the different components within a specific die and package system. The cycling test system has a cold dwell at -65°C and a hot dwell 150°C,and it employs a circulating air environment to ensure rapid stabilization at a specified temperature. During temperature cycling test, devices are inserted into the cycling test system and held at cold dwell for 10 minutes, then the devices are heated to hot dwell for 10



minutes. One cycle includes the duration at both extreme temperature and the two transition times.

The transition period is less than one minutes at 25°C Samples of surface mount devices must first undergo preconditioning and pass a final electrical test prior to the temperature cycling test.

| Test Item | Test Condition | Test Time |
|-----------|--|-----------|
| TCT |  | 500Cycles |

3.3.2.6 Solderability Test

The purpose of this method is to provide a means of determining the solderability of device package terminations that are intended to be joined to another surface using lead-(pb-) containing or pb-free solder for the attachment.

| Test item | Test Condition | Sample | Status |
|---------------|--------------------------|--------|--------|
| Solderability | Steam aging:8H;245°C, 5s | 15 | Pass |

3.3.3 Test Criteria and Result

The following table shows the test results and reference standard of environmental test. The test status and results of TL9527BER are also presented in the table. All pass from these test results mean that Telink products are much more durable in most of their service environment.

| Test Item | Reference Standard | A/R Criteria | Failure/S.S | Status | Failure Mode |
|----------------------|--------------------|--------------|-------------|--------|--------------|
| Moisture Sensitivity | JESD22-A113 | 0/1 | 0/308*1 | Pass | NA |
| HTST | JESD22-A103 | 0/1 | 0/77*1 | Pass | NA |
| TCT | JESD22-A104 | 0/1 | 0/77*1 | Pass | NA |
| PCT | JESD22-A102 | 0/1 | 0/77*1 | Pass | NA |
| UHA | JESD22-A118 | 0/1 | 0/77*1 | Pass | NA |
| SD | JESD22-B102 | 0/1 | 0/15*1 | Pass | NA |



3.4 Package characterization

The purpose of bond pull test is to measure bond strengths, evaluate bond strength distributions, or determine compliance with specified bond strength requirements of the applicable acquisition document. This test may be applied to the wire-to-die bond, wire-to-substrate bond, or the wire-to-package lead bond inside the package of wire-connected microelectronic devices bonded by soldering, thermocompression, ultrasonic, or related techniques. It may also be applied to bonds external to the device such as those from device terminals-to-substrate or wiring board or to internal bonds between die and substrate in non-wire-bonded device configurations such as beam lead or flip chip devices.

The wire bond shear test is destructive. It is appropriate for use in process development, process control and/or quality assurance.

| Test Item | Reference Standard | A/R Criteria | Sample | Status |
|-----------|--------------------|--------------|-------------------|--------|
| BPS | MIL-STD-883 | CPK >1.67 | 30 bonds /5 units | Pass |
| BS | JESD22-B116 | CPK >1.67 | 30 bonds /5 units | Pass |
| PD | JESD22-B100/B108 | CPK >1.67 | 10ea | Pass |

3.5 ESD test

Electrical discharge into semiconductor product is one of the leading causes of devices failure in the customer's manufacturing process. Telink performs the ESD test to ensure that the performance of TL9527BER will not be degraded to an unacceptable level by exposure to a succession of electrostatic discharge. The test methods and test results are show in following table:

| Test Item | Test Method | | | Fail/Pass |
|-----------|--------------------|----------|--------|-----------|
| | Reference Standard | Criteria | Sample | |
| HBM | JESD22A-114 | +/-2KV | 15ea | 0/15 |
| CDM | JESD22C-101 | +/-500V | 6ea | 0/6 |



3.6 Latch-up Test

CMOS products can be prone to over-voltage exceeding the maximum device rating if the parasitic p-n-p-n SCR (Silicon-controlled rectifier) are improperly biased. When the SCR turn on, it draws excessive current and causes products being damaged by thermal runaway. The following table shows the latch-up test method and the test result of no failure.

| Latch-Up | Test Item | Mode | Spec | Class I | Samples | Fail/Pass |
|----------|----------------------------------|----------|---------|---------|---------|-----------|
| | I-Test | Positive | +100mA | I:25° | 3ea | 0/3 |
| | | Negative | -100mA | | 3ea | 0/3 |
| | V _{supply} Over Voltage | Positive | 1.5Vmax | | 3ea | 0/3 |

3.7 NON-VOLATILE MEMORY

The defines the qualification requirement for NVM device. program Post Cycling High Temperature Data Retention (PCHTDR) and Low Temperature Data Retention (LTDR) samples with a topological checkboard pattern where bit is surrounded by its complement. Memory Cycling Endurance (NVCE) must be performed at two temperatures at 25°C and 85°C. It is critical that Error Correction Code (ECC) is turned off.

| Test Item | Reference Standard | A/R Criteria | Failure/S. S | Status | Failure Mode |
|-----------|--------------------|--------------|--------------|--------|--------------|
| NVCE | JESD22-117 | 0/1 | 0/77*3 | Pass | NA |
| PCHTDR | JESD22-117 | 0/1 | 0/77*3 | Pass | NA |
| UCHTDR | JESD22-117 | 0/1 | 0/77*3 | Pass | NA |
| LTDR | JESD22-117 | 0/1 | 0/77*3 | Pass | NA |



4 Conclusion

Reliability test is to ensure the ability of a product in order to perform a required function under specific conditions for a certain period of time. Through those tests, the devices of potential failure can be screened out before shipping to the customer. At the same time, the test results are fed back to process, design and other related departments for improving product quality and reliability.

According to the life time test data, the long-term 1000Hrs failure rate (=the normal operation 1-10 year) of TL9527BER is equal to 36.64 FITS at $T_a=125^{\circ}\text{C}$ and $V_{cc}=3.63\text{V}$ with 60% confidence level and 92.08 FITS at $T_a=125^{\circ}\text{C}$ and $V_{cc}=3.63\text{V}$ with 90% confidence level. The results of environmental test, ESD test and latch-up test also ensure that the TL9527BER is manufactures under a precise control of quality by Telink and its subcontractors. Thus, this experiment based on the Telink reliability test standard for above test items can all pass.

With the extensive research and development activities and the cooperation of all departments, Telink continuously sets and maintains higher standard of quality and reliability to satisfy the future daman of its customers.